CS1101: Lecture 27

The Digital Logic Level: Buses

Dr. Barry O'Sullivan
b.osullivan@cs.ucc.ie

Course Homepage
http://www.cs.ucc.ie/~osullb/cs1101

Lecture Outline

- Buses
- Computer Buses
- Masters & Slaves
- Bus Lines
- Bus Types
- **Reading**: Tanenbaum, Chapter 3, Section 4

Computer Buses

- A **bus** is a common electrical pathway between multiple devices.
- A set of rules called a **bus protocol** describe how a bus is built – mechanical & electrical
- Examples of common bus:
  - IBM PC bus – PC/XT
  - SCSI bus – PCs and Workstations
  - Nubus – Macintosh
  - FireWire – consumer electronics

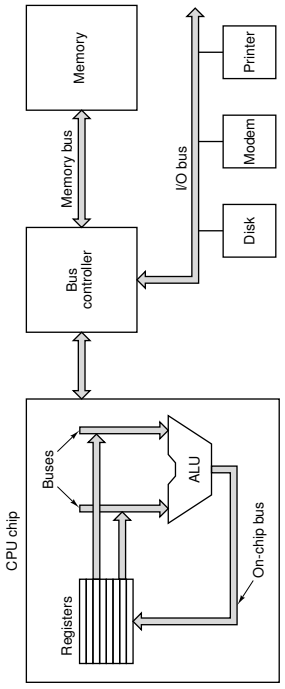

Figure 3-34. A computer system with multiple buses.

Masters & Slaves

- Some devices that attach to a bus are active and can initiate transfers, whereas other are passive and wait for requests.
- The active ones are called **masters**.
- The passive ones are called **slaves**.
- For example, when a CPU orders a disk controller to read or write a block, the CPU is acting as master, and the disk controller is acting as a slave.
- Devices can play many roles.
- Memory is never a master.

Buses

- Bus lines can be divided into address, data and control lines
- There may not be a one-to-one mapping between the CPU pins and the bus signal
- Buses can be divided into two distinct categories: synchronous bus and asynchronous bus
- A **synchronous bus** is driven by a master clock. All bus activities take an integral number of these cycles, called **bus cycles**
- An **asynchronous bus** does not have a master clock. Full handshaking is used to synchronise the slave to the master. Bus cycles can be of any length required and need not be the same between all pairs of devices.