CS1101: Lecture 26

The Digital Logic Level: Memories & CPUs

Dr. Barry O'Sullivan
b.osullivan@cs.ucc.ie

Course Homepage
http://www.cs.ucc.ie/~osullb/cs1101

Lecture Outline

- Memory
  - The S-R Latch
  - RAM
  - ROM
- CPU Chips
  - The Pins of a CPU
  - Control Pins of a CPU
  - Logical pinout of a generic CPU
- **Reading**: Tanenbaum, Chapter 3, Sections 3 & 4

The S-R Latch

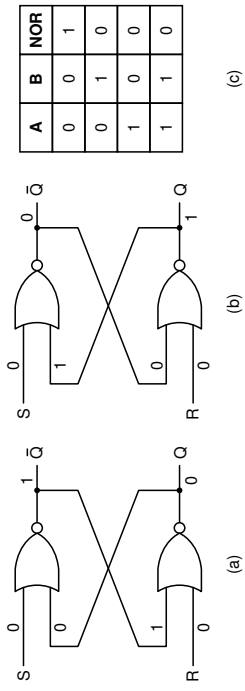

Figure 3-22. (a) NOR latch in state 0. (b) NOR latch in state 1. (c) Truth table for NOR.

SR Latch - Effect of Inputs

- Suppose that S becomes 1 while Q = 0.
- This forces the $\overline{Q}$ output to 0.
- This change makes both inputs to the lower gate 0, forcing the output to 1.
- Thus setting S (i.e., making it 1) switches the state from 0 to 1.
- Setting R to 1 when the latch is in state 0 has no effect because the output of the lower NOR gate is 0 for inputs of 10 and inputs of 11.
- Using similar reasoning, it is easy to see that setting S to 1 when in state Q = 1 has no effect but that setting R drives the latch to state Q = 0.

SR Latch - Summary

- When S is set to 1 momentarily, the latch ends up in state Q = 1, regardless of what state it was previously in.
- Likewise, setting R to 1 momentarily forces the latch to state Q = 0.
- The circuit ”remembers” whether S or R was last on.
- Using this property we can build computer memories.
- Two latch circuits which incorporate clocks are:
  - Clocked SR Latches
  - Clocked D Latches

  The **Clocked D Latch** is a true 1-bit memory.

Memories

- Memories are available as
  - RAM
  - ROM
  - PROM
  - EPROM
  - EEPROM
  - Flash
- We will say a little about each of these in turn

RAM

- Random-Access Memory
- Data stored in RAMs only exists while the computer is powered-up.
- RAMs come in two varieties – static and dynamic
- **Static RAMs** need not be refreshed – they keep their values as long as the power remains on.
- **Dynamic RAMs** must be refreshed periodically to compensate for leakage from the little capacitors on the chip

ROM

- Read-Only Memory
- Data stored in ROMs exists even when the computer is powered-down.
- The contents of ROMs cannot be changed or erased – data is inserted during manufacturing
- To make it easier for companies to develop new ROM-based products, the **PROM** (Programmable ROM) was invented
- A PROM can be programmed once!
- An **EPROM** (Erasable ROM) can be field-programmed and field-written
- **EEPROMs** and **flash memories** are other types of EPROM

CPU Chips and Buses

- All modern CPUs are contained on a single chip
- Each CPU has a set of pins, through which all its communication with the outside world must take place
- Some pins carry signals from the CPU, others accept signals from the outside world, others do both.
- A CPU interacts with the memory and I/O devices at the digital logic level through its pins

The Pins of a CPU

- The pins on a CPU can be divided into three types:
  - Address
  - Data
  - Control
- These pins are connected to similar pins on the memory and I/O chips via a collection of parallel wires called a bus
- Two of the key parameters determining the performance of a CPU are the number of **address pins** and the number of **data pins**
- A chip with m address pins can address up to 2^n memory locations.
- A chip with n data pins can read or write an n-bit word in a single operation.

Control Pins of a CPU

- The control pins regulate the flow of timing of data to and from the CPU and have other miscelaneous uses.
- All CPUs have pins for power, ground and a clock signal.
  - Control pins can be grouped into the following major categories:
  - Bus control
  - Interrupts
  - Bus arbitration
  - Co-processor signalling
  - Status
  - Miscellaneous

Logical pinout of a generic CPU

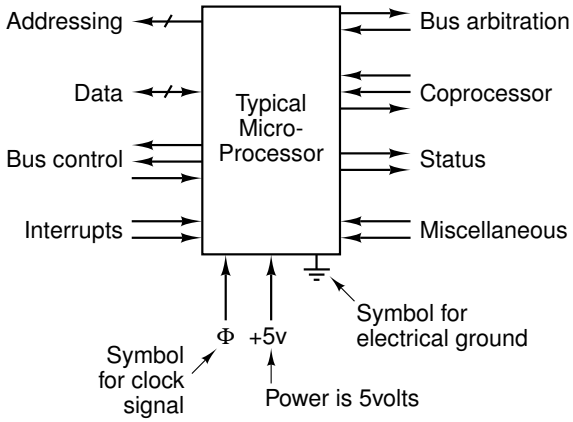

Figure 3-33. The logical pinout of a generic CPU. The arrows indicate input signals and output signals. The short diagonals indicate that multiple pins are used.