

Dr. Menouer Boubekeur

30 years. Married, one child.

Hard/Software Verification Engineer

PhD in Computer science



Dr. Menouer Boubekeur
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Experience

- **Real-Time Systems and Languages:** *Proposal methodologies and prototype realizations for the formal verification of Real-time Systems. (Application to MOQA language)*
 - Evaluation studies for MOQA in the context of a real-time platform (JRTS).
 - Development of a Real-time version of the MOQA language.
- **Formal verification:** *Proposal methodologies and prototype realizations for the formal verification of asynchronous circuits.*
 - Development of a validation environment to verifying asynchronous circuits specifications using enumerative model checking tools.
 - Development of a prototype for the formal verification of asynchronous circuits specifications using symbolic model checking tools.
- **HDL:** Studied & modeled the semantic of VHDL, CHP and SystemC description languages.
- **Design of digital circuits:** Design, simulation, test and synthesis of circuit (VHDL)
- **Industrial project:** Participate at the WUCS project with St-microelectronics (Crolles, France)

Practical skills

Formal verification techniques: Enumerative and symbolic Model-checking, Equivalence checking, Theorem proving.

Formal verification tools & languages: FormalCheck, RuleBase, CADP, Lustre, Esterel, LOTOS, nu-SMV, Lisp, ObjectGeode, ACL2, Omega.

Real-Time Systems: ACET & WCET techniques, Real-Time analysis, Java for Real-Time Systems (JRTS).

Programming languages: JRTS, Java m C, C++, Pascal, Delphi, Builder C++, VBasic, lisp.

VLSI : Design, simulation and synthesis techniques in VHDL. (Synopsys and Mentor Graphics tools), Design and simulation of asynchronous circuits in TAST(CHP) and Tangram tool.

Environments: Windows, Win NT, UNIX, Linux, MacOS,

Microsoft Tools: Word, Powerpnt, Excel, Frontpage

Prototypes demonstration

Presentation of a prototype: "**Formal verification of asynchronous circuits using CHP2IF environment**". DATE 2004. Paris. France.

Presentation of a prototype: "**Formal verification of asynchronous circuits using pseudo-synchronous models**". DATE 2003. Munich. Germany.

Last Degree

00 - 04 **University of Joseph Fourier** **IMAG Institute,** **Grenoble, France**

PhD Thesis in Computer Science at the University of Joseph Fourier. Grenoble. (TIMA laboratory). *Title:* "Formal Validation of Asynchronous Circuits Specifications: Methods and tools". *Thesis Director:* Prof. Dominique Borrione.

Languages

Bilingual: French - Arabic. **English:** Fluent

Work Experiences

- 02/04 - ...** **UCC, CEOL centre** **Cork, Ireland.**
Applied research: Real time systems and languages: application of formal verification techniques in the real time context.
- 10/00 - 10/2004** **TIMA Laboratory** **Grenoble, France.**
Applied research: Proposal methodologies and prototype realizations for the formal verification of asynchronous circuits.
- 10/97 - 07/99** **Adem Info,** **Oran, Algeria**
 Computer Science Engineer, Formation and software development (C++, Delphi).

Selected Publications *(more publications could be find in my personal web site)*

Book Chapters and International journals

- 1) M. Boubekeur, D. Hickey, J. Mc Enery and M. Schellekens, "A new Approach for Modular Average-Case Timing of Real-Time Java Programs", WSEAS Transactions on Computers, Issue2, Volume 1, December 2006, ISSN: 1991-8755.
- 2) D. Borrione, M. Boubekeur, et al. "VLSI-SOC: From Systems to Chips". Chapter: "Validation of Asynchronous Specifications using IF/CADP", Kluwer-Springer, 2006, ISBN: 0-387-33402-5
- 3) D. Borrione, M. Boubekeur, et al. "VLSI-SOC: From Systems to Chips". Chapter: "Validation of Asynchronous Specifications using IF/CADP", Kluwer-Springer, 2006, ISBN: 0-387-33402-5
- 4) M. Boubekeur, D. Borrione, et al. "Languages for System Specifications. Selected Contributions on UML, SystemC, System Verilog, Mixed-Signal Systems, and Property Specifications from FDL'03". Chapter: "Modelling CHP descriptions in Labelled Transition Systems for an efficient formal validations of asynchronous circuit specifications" Ed. Grimm, Christoph. Kluwer Academic Publishers, 2004. ISBN: 1-4020-7991-5.

International Conferences

- 5) M. Boubekeur, D. Hickey, J. Mc Enery and M. Schellekens, "Towards Modular Average-Case Timing in Real-Time Languages: An Application to Real-Time Java". 6th WSEAS International Conference on APPLIED COMPUTER SCIENCE (ACS'06), Tenerife, December, 2006.
- 6) M. Boubekeur, K. Man and M. Schellekens, "Formal Verification of Mutual Exclusion between the Guards of Deterministic Choice Structures". 20th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE 2007), 22-26 April 2007, Vancouver, Canada.
- 7) M. Boubekeur, D. Hickey and M. Schellekens, "Evaluation of MOQA Average-Case Timing Results on a Real Time Platform", Proc of the conference Information of MFCSIT'06, Cork, August 2006.
- 8) M. Boubekeur, D. Borrione, et al. "Modeling CHP descriptions in Labeled Transitions Systems for an efficient formal validation of asynchronous circuit specifications". Publ. in Forum on specification and Design Languages (FDL'03), Frankfurt, Germany, September 23-26, 2003. Selected best papers.
- 9) D. Borrione, M. Boubekeur, et al. "Validation of asynchronous circuit specifications using IF/CADP". Publ. in 12th IFIP International Conference on Very Large Scale Integration (VLSI'03), Darmstadt, Germany, December 1-3, 2003. Selected best papers.
- 10) D. Borrione, M. Boubekeur, et al. "An approach to the introduction of formal validation in an asynchronous circuit design flow". Publ. in 36th Hawai International Conference on Systems Science (HICSS'03), Hawai, USA, January 6-9, IEEE, 2003.

Thesis

- 11) Menouer Boubekeur, "**Formal Validation of Asynchronous Circuits Specifications: Methods and Tools**". PhD Thesis in Computer Science, University of Joseph Fourier. 2004. Grenoble. France.
- 12) Menouer Boubekeur, "**Outils d'aide à la vérification formelle de systèmes infinis**". Master Thesis in Computer Science, University of Joseph Fourier. 2000. Grenoble. France.