Transistors

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February 4, 2013

1 The Bipolar Junction Transistor

We have already considered the diode formed from the juxtaposition of n-type and p-type semiconductors so that a single junction is formed while preserving the continuity of the lattice structure.

When two junctions are created, the resulting device is called a *transistor*. There are two main types of transistor, Bipolar Junction Transistors (BJT) and Field Effect Transistors (FET). We first consider the BJT. There are two ways in which two junctions can be formed: by sandwiching a section of n-type semiconductor between two p-type sections (a pnp BJT) or by sandwiching a section of p-type semiconductor between two n-type sections (an npn BJT). We will concentrate on npn BJTs as they are more common in digital logic applications. Here, one n section is known as the collector (C), one n section as the emitter (E) and the p section is the base (B).

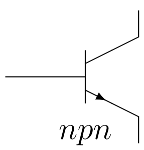


Figure 1: npn BJT

There are three ways of connecting a transistor in a circuit: common base, common collector and common emitter. The common emitter configuration

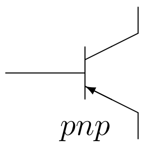


Figure 2: pnp BJT

is most usual; in this, the emitter is connected to ground (common), the input signal is between the base and the emitter and the output signal is between the collector and the emitter.

Consider the biasing arrangements for the two pn junctions, BE and BC. As either junction may be forward or reverse biased, there are four possibilities. If both junctions are reversed biased, all currents are zero (this is an approximation, as there will be small leakage currents across the reverse biased unctions, but we ignore these). In this case, the transistor is said to be in *cutoff*. Viewed as a switch, the transistor can be considered to be OFF.

If the BE junction is forward biased and the BC junction is reverse biased the transistor operates in its *forward active region*. For most transistors in this region, the base current is very small and the emitter and collector currents are approximately equal. Small variations in the base current will lead to relatively large variations in the collector current, a phenomenon that can be used to yield signal amplification in analogue circuits.

If the BE junction is reverse biased and the BC junction is forward biased, the transistor operates in its *reverse active region*. However, this biasing mode is rarely used and we will not discuss it further.

If both the BE and BC junctions are forward biased, the collector current will not be influenced significantly by the base current. The transistor is said to be in *saturation*, where it is conducting its maximum current level. Viewed as a switch, the transistor can be considered to be fully ON.

1.1 Switching

If V_{BE} is less than a critical level, called the cut-in, $V_{BE\gamma}$, the base current is zero, resulting in I_C=0 and the transistor is in cutoff.

If V_{BE} is greater than a second threshold, above the cut-in, the transistor is turned on and I_C rises to its saturation value.

For digital switching (0-1 interpretation), we are interested only in the cutoff and saturation modes of transistor operation.

In cutoff, the main criterion is $V_{BE} < V_{BE\gamma}$. We assume that the collector voltage is more positive than the base voltage. In digital logic, we use $V_{BE\gamma} = 0.5\text{V}$.

In saturation, $I_B > 0$ and we use $V_{BE} = 0.8\text{V}$ and $V_{CE} = 0.2\text{V}$.

1.2 Inversion

Consider a resistor connected between V_{CC} and the collector. If the input voltage is
$V_{LO} = V_{BE} < V_{BE\gamma}$,
$I_C = 0$ and therefore $V_R = 0$ and $V_C = V_{CC} > V_{HI}$.

If the input voltage is
$V_{HI} = V_{BE} > 0.8\text{V}$,
$V_R = V_{CC} - V_{CE}$ and $V_{CE} = 0.2\text{V} < V_{LO}$.

Thus the transistor acts as a logic inverter.

2 The Field Effect Transistor

The modern incarnation of the field effect transistor is the MOSFET (Metal Oxide Semiconductor Field Effect Transistor). There are two types of MOSFET, n-channel MOS (nMOS) and p-channel MOS (pMOS). Both types are combined in CMOS (Complementary MOS) circuitry.

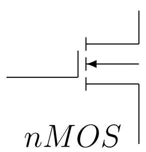


Figure 3: n-channel MOSFET

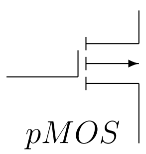


Figure 4: p-channel MOSFET

Consider a schematic of an n-channel MOS device. There is a substrate of p-type Si into which two n-type regions have been diffused to form the source (S) and drain(D). The channel region between S and D is covered with an insulating layer of SiO_2. A metal layer on top of the SiO_2 acts as a gate (G). A voltage applied between S and D will reverse bias one of the pn junctions and no current will flow.

Suppose the source of an n-channel MOSFET is connected to ground and the drain and gate are connected to $+V_{DD}$ and $+V_{GG}$ respectively, in a frequently-used connection mode known as common-source. If V_{GG} is positive enough, electrons are attracted from within the p-type substrate to the vicinity of the gate. As the gate is insulated, no current flows through it and the electrons gather below the gate, forming an n-type channel in the substrate. Current is able to flow from drain to source through the channel. As V_{GG} rises, more electrons accumulate below the gate and channel conductance is increased. For a particular value of V_{GG}, I_D increases in proportion to V_{DS}. However, the cross-section of the channel is not uniform; it decreases from source to drain. Eventually, if V_{GG} becomes sufficiently high, a region of MOSFET operation known as *pinchoff* is reached. Increasing V_{GG} beyond this point yields no further increase in I_D.

Thus, there are three regions of MOSFET operation. Before V_{GG} is positive enough, the device is in *cutoff.* Beyond cutoff, channel conductance varies with V_{GG} and drain current rises in proportion to V_{DS}. Here, the channel behaves like a variable resistor and the MOSFET is in its *triode region.* The third region is *pinchoff*, which is analogous to the phenomenon of saturation in BJTs.

We are interested in MOSFETS as switching devices, so the interesting device operating regions are cutoff and pinchoff.

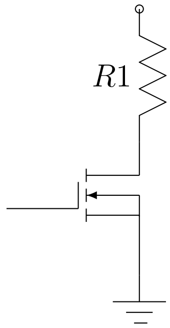
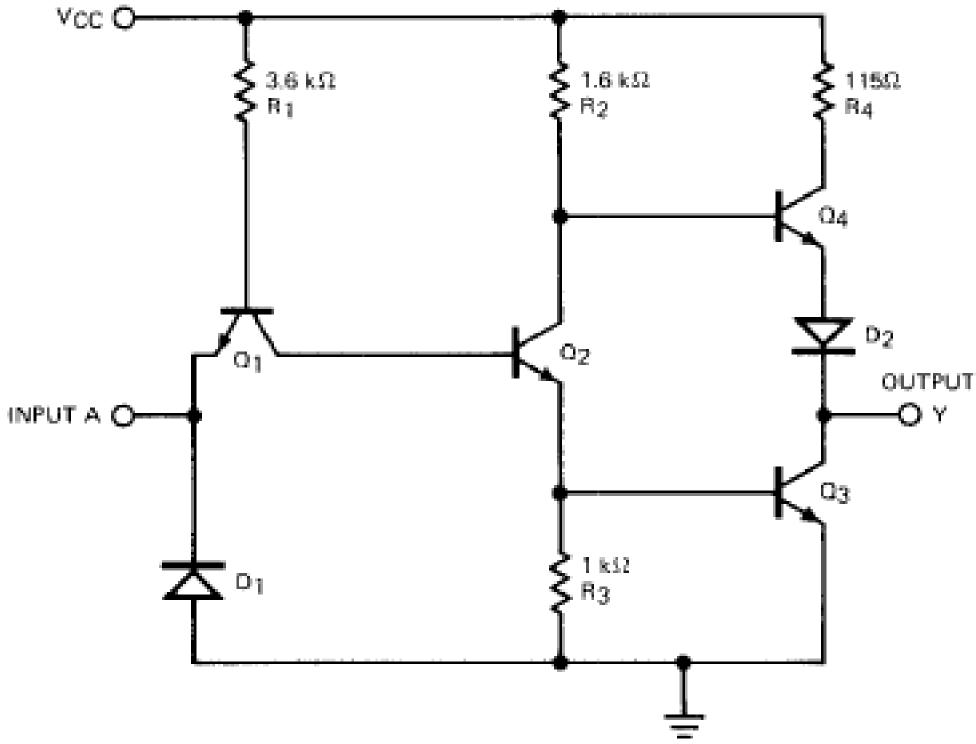
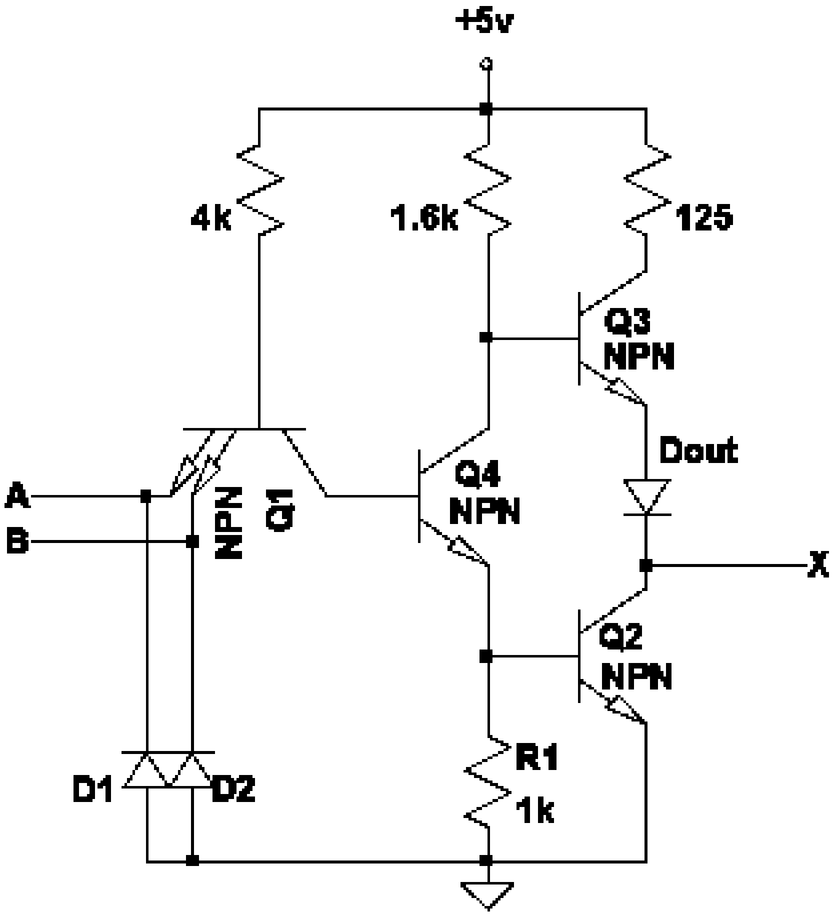


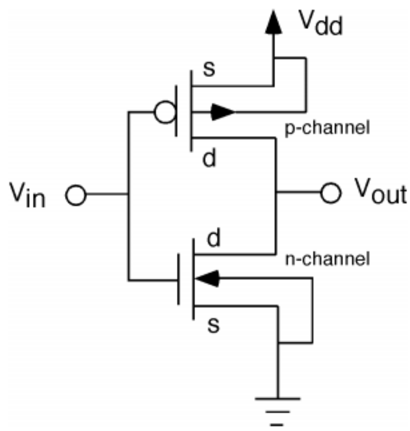
Figure 5: n-channel switch

3 Circuits



VCC
3.6 kΩ
R1
1.6 kΩ
R2
115Ω
R4
Q4
Q1
Q2
D2
OUTPUT
INPUT A
Y
Q3
D1
1 kΩ
R3





inverter.png

CMOS NAND gate