

**Ollscoil na hÉireann
The National University of Ireland**

**Coláiste na hOllscoile, Corcaigh
University College, Cork**

Final Examination 2014

CS6323 Complex Networks and Systems

M.Sc. Software and Systems for Mobile Networks
M.Sc. Computer Science

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Attempt all questions

Total marks: 100

60 minutes

Please answer all questions
Points for each question are indicated by [xx]
(Each question should be allocated roughly 15 minutes)

1. **[25]** The company Amazon wants to calculate the number of times customers ordered pairs of goods at the same time. For a set of goods $G=\{G_1, G_2, \dots, G_m\}$, and a set of customer orders $O=\{O_1, O_2, \dots, O_n\}$, with $n>m$, Amazon wants to know the number of times customers ordered multiple items from G in an order in the set O of orders. We have up to n^2 CPUs available for processing at any time.
 - a) **[5]** Draw a figure showing the architecture of using MapReduce for solving the Amazon problem.
 - b) **[10]** Write out the pseudo-code for applying MapReduce to compute when customers ordered any two items together. In other words, we want to return the vector $\{(G_1, \Omega_1), (G_2, \Omega_2), \dots, (G_m, \Omega_m)\}$, where Ω_i is the number of times good $G_i \in G$ was ordered with one other good.
 - c) **[10]** Extend this to compute the number of times a customer ordered *three or more goods* containing G_i (denoted $\#_i$), for each $G_i \in G$. In other words, we want to return the vector $\{(G_1, \#_1), (G_2, \#_2), \dots, (G_m, \#_m)\}$.

2. **[25]** A network designer wants to compare the performance and reliability of two systems: a triple-modular-redundant (TMR) system and a dual-dual-redundant (DDR) system, as shown in Figure 1. In the TMR system, each processor has service rate $\mu=25$ packets/s, and the voter (V) has service rate 100 packets/s. The TMR system has input rate of $\lambda=60$ packets/s. The DDR system $\lambda=60$ packets/s, each processor has service rate $\mu=20$ packets/s, and the voter (V) has service rate of either 50 or 100 packets/s, as shown in Figure 1(b). The input streams are split as shown in the figure. We assume that all input and processing rates are exponentially distributed. The expected waiting time is $W = 1/(\mu - \lambda)$. The TMR system works if 2 out of 3 CPUs is OK, and a DDR module works if 1 out of 2 CPUs is OK.
 - a. **[10]** Compare the throughput times for the two designs.
 - b. **[10]** If each CPU fails with fixed probability 0.01, and the voter V never fails, compare the reliability of the two designs.
 - c. **[5]** If the TMR system works if 2 out of 3 CPUs are OK, and we have reward of 10 if the system is OK and reward 0 otherwise, compute the expected reward for this TMR system.

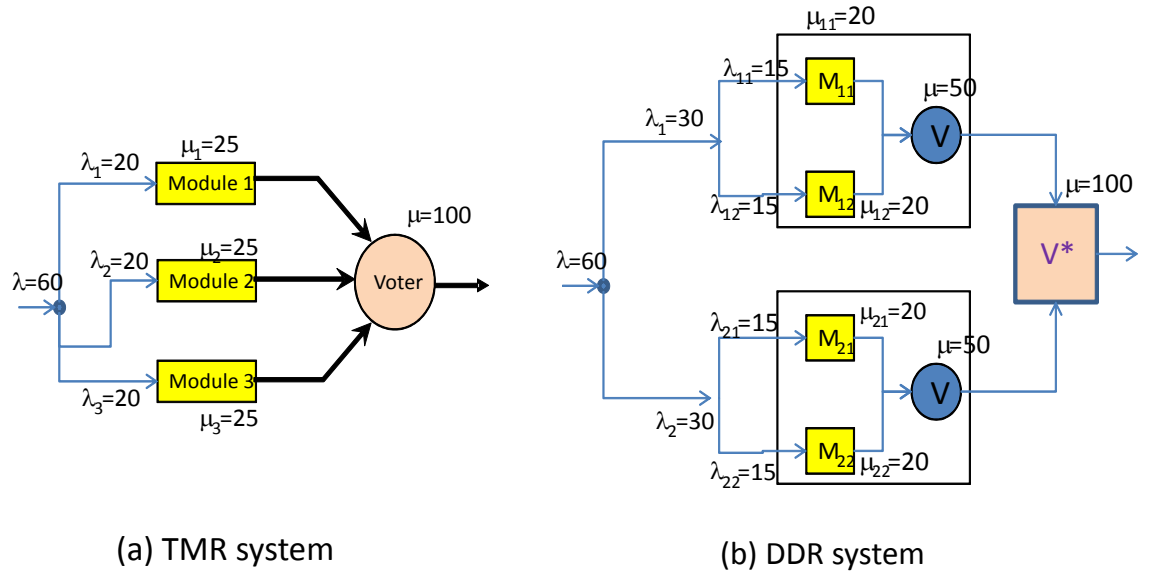


Figure 1: TMR and Dual-dual (DDR) fault-tolerant network configurations

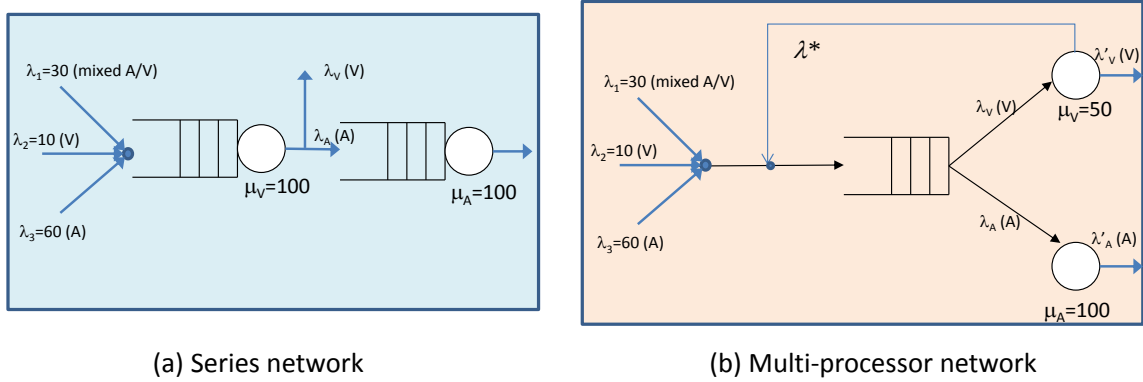


Figure 2: Architectures for computer network, with series (a) and multi-CPU (b) designs

3. [20] A chip manufacturer is designing a multi-core CPU to process video (V) and arithmetic (A) packets. Figure 2 shows the 2 possible designs. The input stream consists of 3 types of packets: (i) packets with mixed video/arithmetic content; (ii) packets with video (V) content only; (iii) packets with arithmetic (A) content only. A packet with mixed video/arithmetic content must be processed by both the video and arithmetic CPUs. We assume that all input streams and all processing are exponentially distributed. The input rates and processor rates (packets per hour) are shown in Figure 2.

Design (a) has a video processor in sequence with an arithmetic processor. λ_V denotes the rate of packets with video content only, and λ_A denotes the rate of packets with some arithmetic content. Packets with arithmetic content only pass straight through the video processor to be processed by the arithmetic processor. The video processor performs computations on all packets with video or mixed video/arithmetic content, and then send packets with mixed video/arithmetic content to the arithmetic processor following video processing. Design (b) has a two-CPU processor with single input buffer, where the video processor takes care of all packets with video content, but

must send packets with mixed video/arithmetic content back as input for the arithmetic content to be dealt with by the arithmetic processor.

- a) [15] Compare the throughput times for the series and multi-processor designs.
 - b) [5] If we choose to double to speed of the video processing CPU, which design is most affected?
4. [30] Consider again the network shown in Figure 2. We assume that both video and arithmetic modules can fail.
- We assume that we obtain revenue of €100/packet (either video or audio or mixed content) if the system functions properly. Both video (V) and audio (A) modules fail at rate 1/day, and are repaired at rate 99/day.
- (a) [15] Draw a Markov model for failure and repair of video (V) and audio (A) modules (assuming that both A and V can be repaired simultaneously), and derive the failure distribution, e.g., $\Pr(A=\text{fail} \ \& \ V=\text{fail})$, $\Pr(A=\text{OK} \ \& \ V=\text{OK})$, etc. for each of the two designs.
 - (b) [5] Define the system failure states for both designs in terms of the failure status of the video (V) and audio (A) modules. A system is *OK* if it achieves its full throughput rate, degraded if it has less than full throughput rate, and is failed if it has no throughput.
 - (c) [10] Compute the expected revenue/day for the series network design.